免电感滤波2*20W D类立体声音频功放

■ 特点

- 输出功率（BTL模式）
  2×20W (V_{DD}=14.5V, R_L=4Ω, THD+N=1%)
  2×25W (V_{DD}=14.5V, R_L=4Ω, THD+N=10%)
- 输出功率（PBTL模式）
  24W (V_{DD}=15V, R_L=4Ω, THD+N=1%)
  30W (V_{DD}=15V, R_L=4Ω, THD+N=10%)
- 单电源系统，4.5V-16V宽电压输入范围
- 超过90%效率，无需散热器
- 可选输出模式：BD和1SPW
- 扩频功能，免电感滤波
- 模拟差分/单端输入，输出模式立体声/单声道可选
- 可选增益：32dB/17.6dB
- 保护功能：过压/过流/过热/欠压异常，直流检测和短路保护
- 无铅无卤封装，TSSOP28-PP

■ 应用

- 条形音箱
- 便携式音箱
- 拉杆音箱
- 无线智能音箱
- 消费类音频应用
- LCD电视/监视器

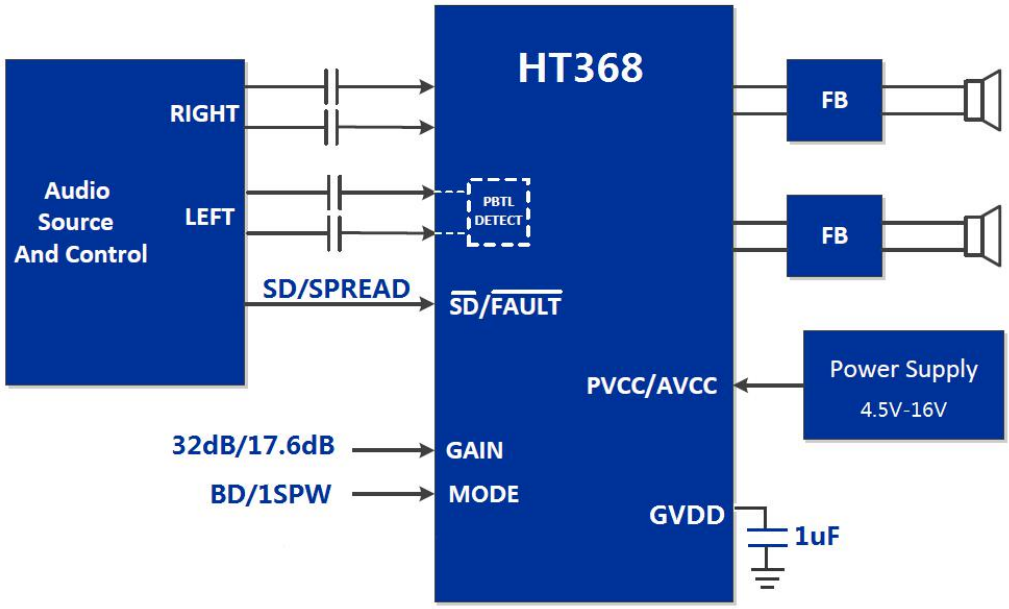
■ 概述

HT368是一款高效D类音频功率放大器。在14.5V供电的立体声（BTL）模式下，能够持续提供2*20W/4Ω功率输出；在单声道（PBTL）模式下，能够持续提供30W/4Ω功率输出。

HT368具有先进的扩频功能来抑制EMI，使用价格低廉且小体积铁氧体磁珠可满足EMC要求。

此外，HT368内置关断功能使待机电流最小化，还集成了过压保护、直流保护、短路保护、热保护和电源欠压异常保护等功能，可全面防止出现故障。

■ 简化应用图



TEL:0755-82863877 13242913995 E-MAIL:panxia168@126.com http://www.szczkjgs.com

2*20W Inductor Free Class D Stereo Amplifier

■ FEATURE

- Output Power (BTL)
  2×20W (V_{DD}=14.5V, R_L=4Ω, THD+N=1%)
  2×25W (V_{DD}=14.5V, R_L=4Ω, THD+N=10%)
- Output Power (PBTL)
  24W (V_{DD}=15V, R_L=4Ω, THD+N=1%)
  30W (V_{DD}=15V, R_L=4Ω, THD+N=10%)
- Single Wide Voltage Supply: 4.5V-16V
- Selectable Work Mode: BD or 1SPW
- Efficiency > 90%
- Differential / Single-ended Analog Input, BTL or PBTL Output
- Selectable Gain: 32dB or 17.6dB
- Spread Switching Frequency For Inductor Free
- Integrated Self-protection Circuits Including Overvoltage, Undervoltage, Overtemperature, DC-detect, and Overcurrent with Error Reporting
- LF and HF Package of TSSOP28-PP

■ APPLICATIONS

- Sound Bars
- Wireless Speakers
- Consumer Audio Applications
- TVs/Monitors

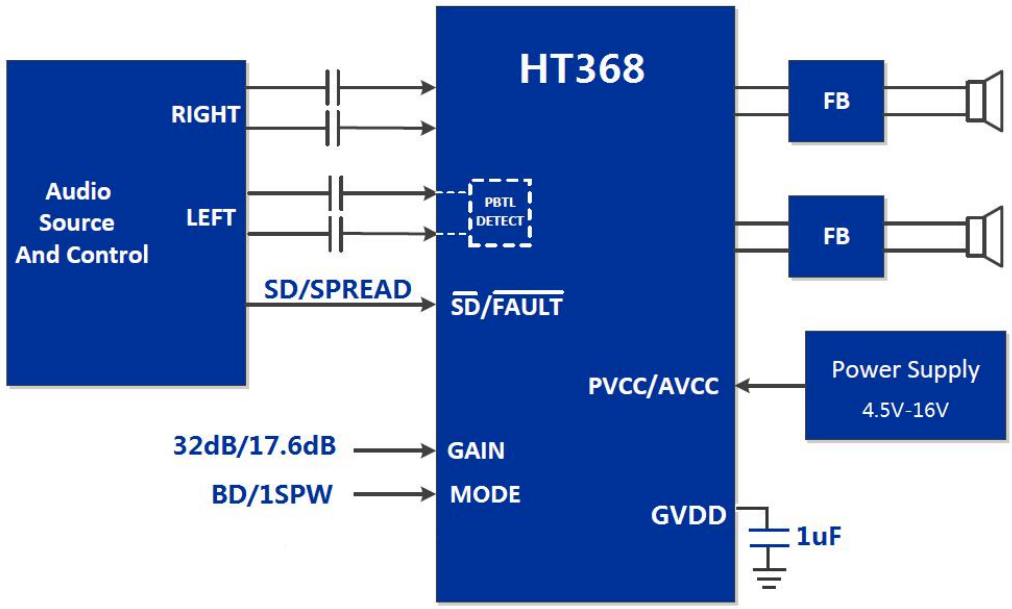
■ GENERAL DESCRIPTION

HT368 is a stereo efficient, Class-D audio amplifier for driving speakers up to 30W/4 Ω in mono PBTL. It can also deliver 2×20W/4Ω power in stereo BTL.

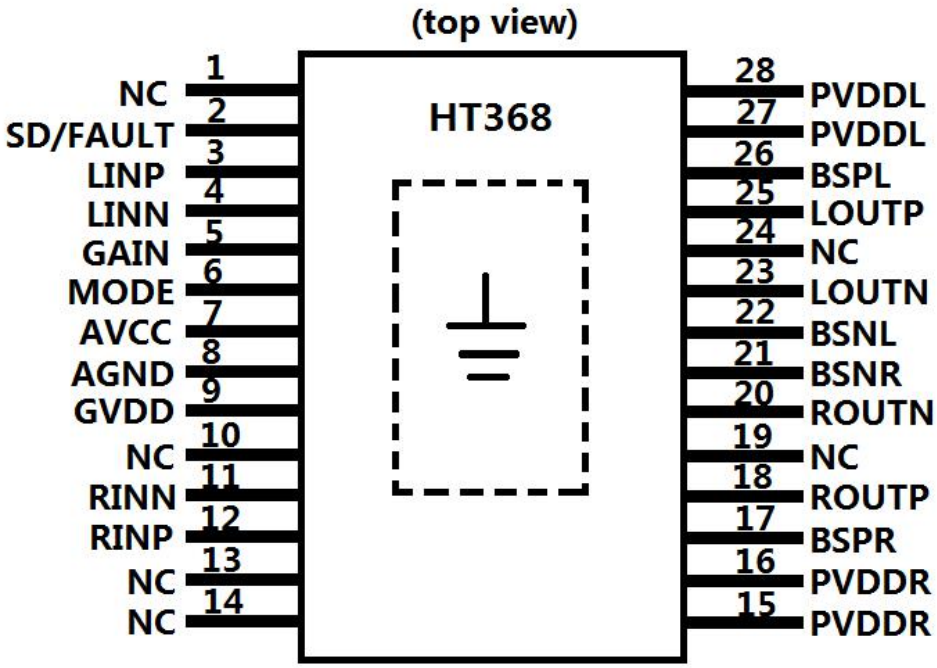
Advanced EMI Suppression with Spread Spectrum Control enables the use of inexpensive ferrite bead filters while meeting EMC requirements for system cost reduction.

HT368 is fully protected against faults with Overvoltage, Undervoltage, Overtemperature, DC-detect, and Overcurrent protection. Faults can be reported to the processor to prevent devices from being damaged

■ TYPICAL APPLICATION



■ TERMINAL CONFIGURATION



Pin No.	Name	I/O[1]	Description
2	\SD/FAULT	I	SD/FAULT, multi function pin. When pulled down, place the speaker amplifier in shutdown mode. General fault reporting including Over-Temp, Over-Current, DC Detect.
3	LINP	I	Positive input terminal for L channel
4	LINN	I	Negative input terminal for L channel
5	GAIN	I	Gain select pin. Low = 17.6dB gain; High or float = 32dB
6	MODE	I	Mode select pin. Low = BD; High or float = Low-Idle-Current 1SPW
7	AVCC	P	Analog power supply.
8	AGND	G	Analog signal GND. Connect to PGND.
9	GVDD	O	Voltage regulator derived from AVDD supply, connect 1uF to GND
11	RINN	I	Negative input terminal for R channel
12	RINP	I	Positive input terminal for R channel
15/16	PVDDR	P	Power Supply for amplifier drivers of R channel
17	BSPR	BST	Connection point for the ROUTP bootstrap capacitor, which is used to create a power supply for the high-side gate drive for ROUTP
18	ROUTP	O	Positive pin for differential speaker amplifier output R
20	ROUTN	O	Negative pin for differential speaker amplifier output R
21	BSNR	BST	Connection point for the ROUTN bootstrap capacitor, which is used to create a power supply for the high-side gate drive for ROUTN
22	BSNL	BST	Connection point for the LOUTN bootstrap capacitor, which is used to create a power supply for the high-side gate drive for LOUTN
23	LOUTN	O	Negative pin for differential speaker amplifier output L
25	LOUTP	O	Positive pin for differential speaker amplifier output L
26	BSPL	BST	Connection point for the LOUTP bootstrap capacitor, which is used to create a power supply for the high-side gate drive for LOUTP
27/28	PVDDL	P	Power Supply for amplifier drivers of L channel
PAD	PGND	G	Power ground, make sure connect it to the system ground
1/10/13/ 14/19/24	NC		NC

[1] I: Input; O: Output; G: Ground; P: Power; BST: Boot Strap

■ ORDERING INFORMATION

Part Number	Package Type	Marking	Operating Temperature Range	MOQ/Shipping Package
HT368MTET	TSSOP28L-PP	HT368MTE UVWXYZ [1]	-40℃～85℃	30PCS / Tube
HT368MTER	TSSOP28L-PP	HT368MTE UVWXYZ [1]	-40℃～85℃	2500PCS / Tape

[1] UVWXYZ is production tracking code

■ SPECIFICATIONS[1]

● Absolute Maximum Ratings[2]

PARAMETER	Symbol	MIN	MAX	UNIT
Supply voltage range (PVDD,AVDD)	PV_{DD}	-0.3	18	V
Input voltage range (LINP, LINN, RINP, RINN)	V_I	−0.3	5.8	V
Input voltage range (\SD, MODE, GAIN)	V_I	−0.3	AVDD	V
Operating temperature range	T_A	-40	85	℃
Operating junction temperature range	T_J	-40	150	℃
Storage temperature range	T_{STG}	-50	150	℃

● Recommended Operating Conditions

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Supply voltage range	V_{DD}	PVDD,AVDD	4.5		16	V
Operating temperature	T_a		-40	25	85	℃
High-level input voltage	V_{IH}	\SD, Spread on	2.5		AVDD	V
Middle-level input voltage	V_{IM}	\SD, Spread off	1.5		2.2	V
Low-level input voltage	V_{IL}	\SD			0.8	V
High-level input voltage	V_{IH}	GAIN, MODE	1.5		AVDD	V
Low-level input voltage	V_{IL}	GAIN, MODE			0.8	V
Low-level output voltage	V_{OL}	FAULT, OPEN-DRAIN OUTOUT			0.5	V
Load impedance (BTL)	R_L	With output filter	3.2	4		Ω
Load impedance (PBTL)	R_L	With output filter	1.6	2		Ω

● DC Electrical Characteristics

Conditions: T_A = 25℃, PV_{DD} = 4.5-16V, Load = 4ohm, unless otherwise specified.

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Class Output Offset Voltage	V_{OS}	V_I = 0V, Gain = 32dB		1.5		mV
Quiescent supply current	I_{DD}	V_{DD} = 12V, No Load		12		mA
Quiescent supply current in SD mode	I_{SD}	V_{DD} = 12V, With Load		12		uA
System Gain in BTL or PBTL mode	Gain	GAIN=H, Rin = 0kΩ		32		dB
		GAIN=H, Rin = 8.2kΩ		26		dB
		GAIN=L, Rin = 0kΩ		17.6		dB
Turn-on time	t_{on}	Pull \SD high or power on		90		ms
Turn-off time	t_{off}	Pull \SD low		5		us
Gate drive supply	GVDD			5		V

[1] Depending on parts and PCB layout, characteristics may be changed.

[2] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

● AC Electrical Characteristics

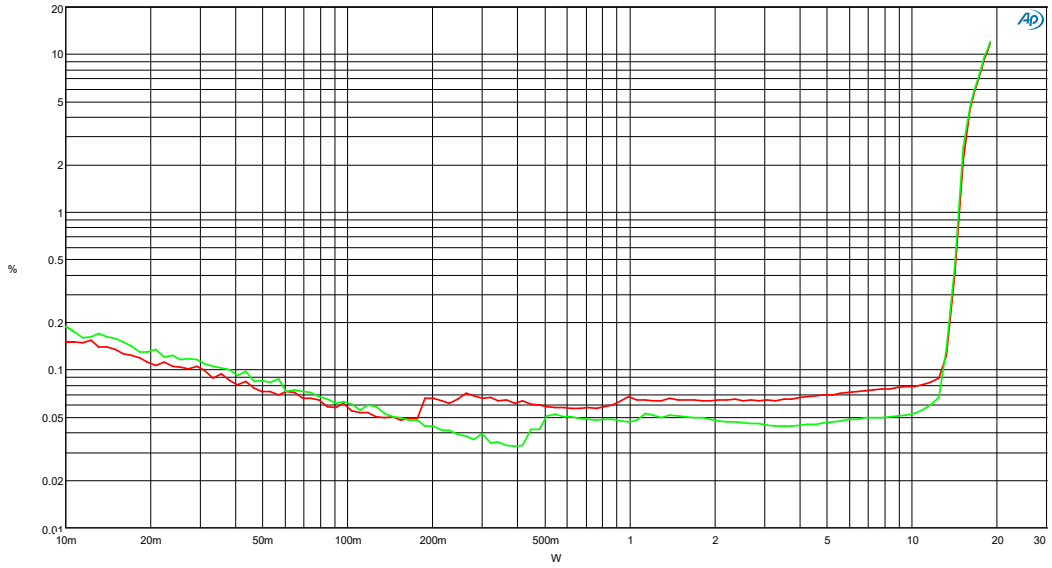
Conditions: T_A = 25℃, V_{DD} = 4.5-16V, Load = Filter + R_L, Filter = 300R Bead + 1nF, R_L = 4Ω + 22uH, f_{IN} = 1 kHz, Gain = 26dB, C_{IN} = 1uF, 20-20kHz, unless otherwise specified.

PARAMETER	Symbol	CONDITION		MIN	TYP	MAX	UNIT
Continuous output power	P_O	BTL, VDD = 12V, R_L = 4Ω+22uH,	THD +N = 1%		14		W
			THD+N = 10%		17		W
		BTL, VDD = 12V, R_L = 8Ω+33uH,	THD +N = 1%		8		W
			THD+N = 10%		10		W
		VDD = 16V, R_L = 3Ω+22uH, PBTL	THD +N = 1%		35		W
			THD+N = 10%		44		W
		VDD = 16V, R_L = 4Ω+22uH, PBTL	THD +N = 1%		28		W
			THD+N = 10%		35		W
Total harmonic distortion + noise	THD+N	Po = 1W, V_{DD} = 12V, R_L = 4Ω			0.05		%
Efficiency	η	VDD = 12V, THD+N = 10%	R_L = 4Ω, BTL		88		%
			R_L = 8Ω, BTL		93		%
Cross Talk	CT	Po = 1W, Gain = 26dB			-74		dB
Output integrated noise	V_N	A-weighted, Gain = 17.6 dB			120		uV
Signal-to-noise ratio	SNR	A-weighted, Gain = 17.6 dB, Po = 1W			82		dB
Power supply rejection ratio	PSRR	200mVpp 1kHz, Input grounded			-75		dB
Oscillator frequency	f_{osc}				360		kHz
Spread frequency range					±15		kHz
Over temperature protection trigger point	OTP				160		℃
Thermal holdback trigger point	TFB				150		℃
Over current trip point	OCP				7.5		A

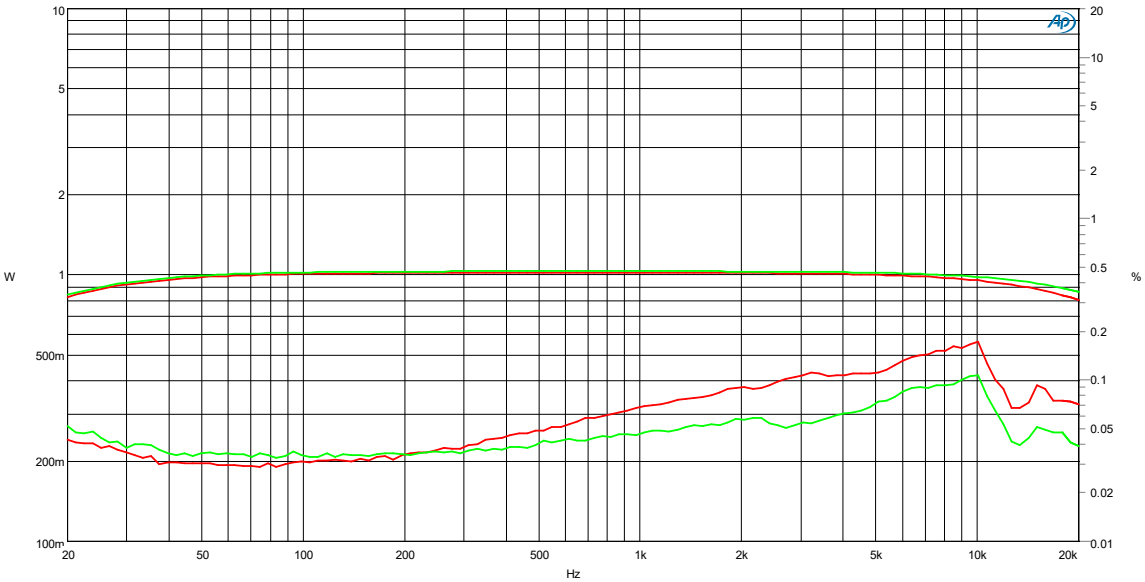
■ TYPICAL OPERATING CHARACTERISTICS

BTL

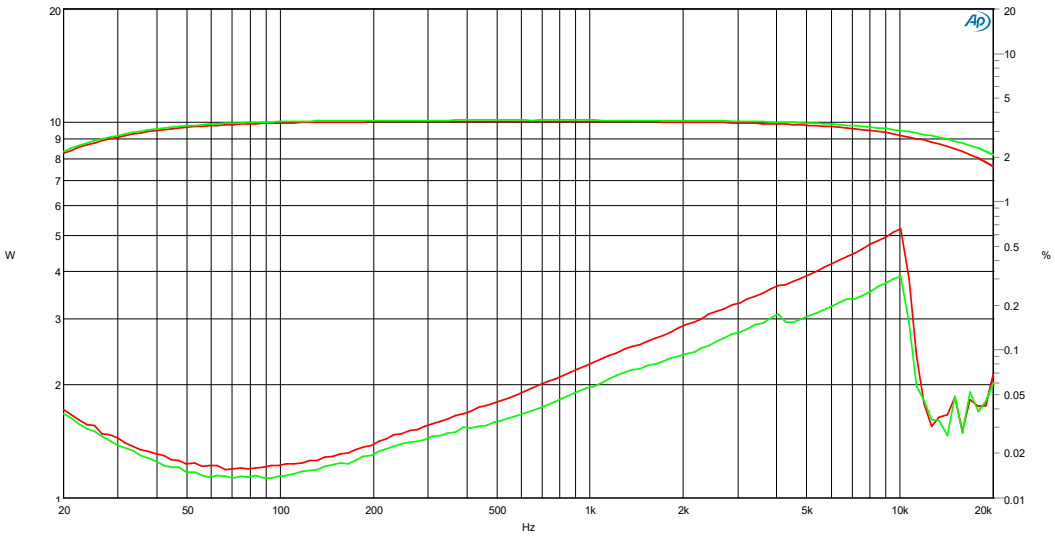
Condition: PVDD = 12V, f_{IN} = 1kHz, C_{IN} = 1uF, MODE=H, GAIN=H, external R_{IN} = 8.2kohm, RL=4R, unless otherwise specified



Output Power vs THD+N

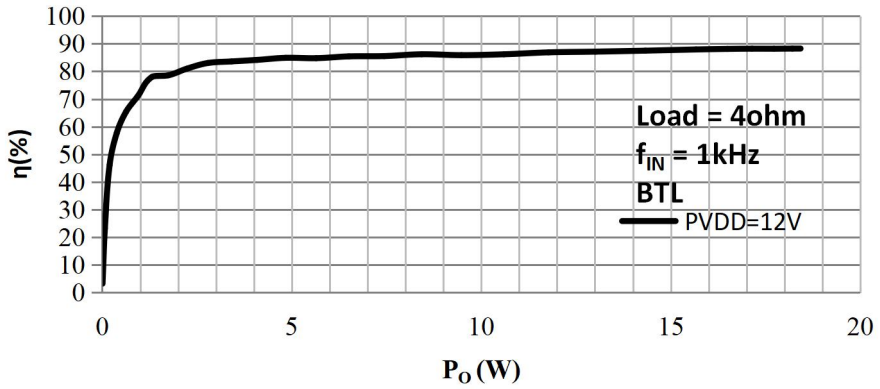


f_{IN} vs THD+N(Po=1W)

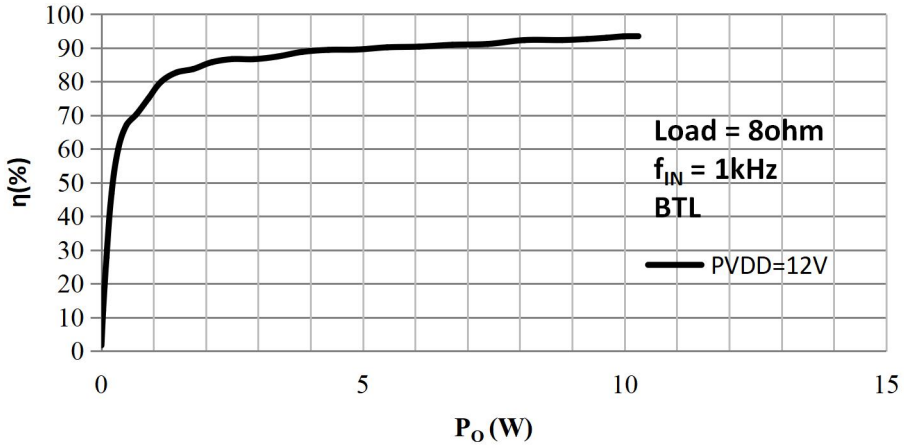


f_{IN} vs THD+N(Po=10W)

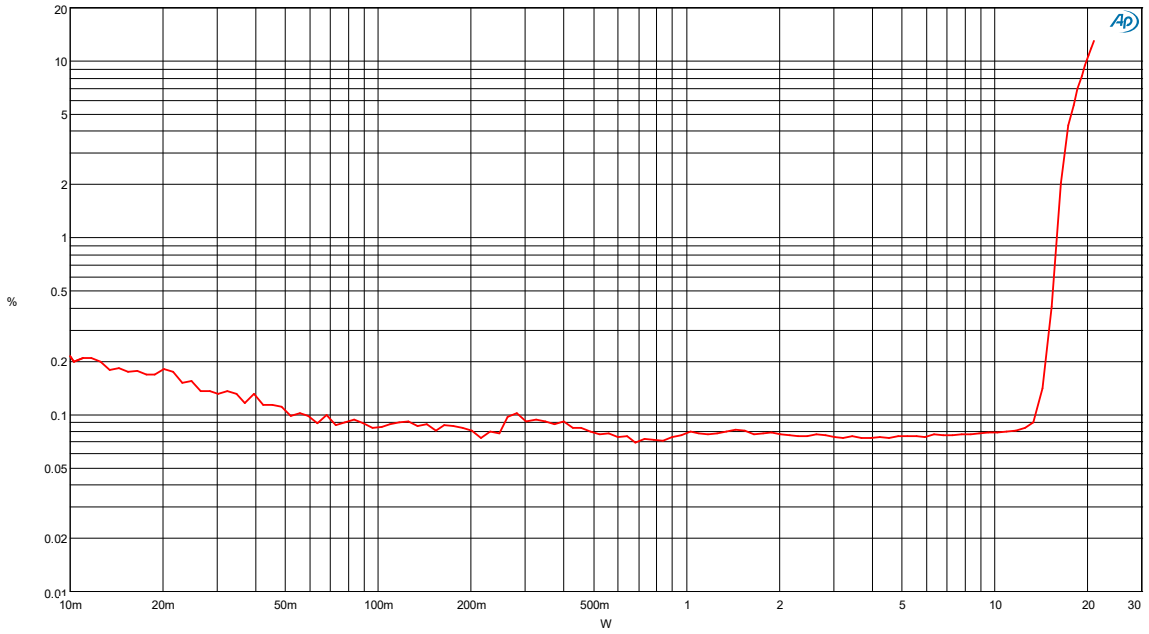
P_O vs η



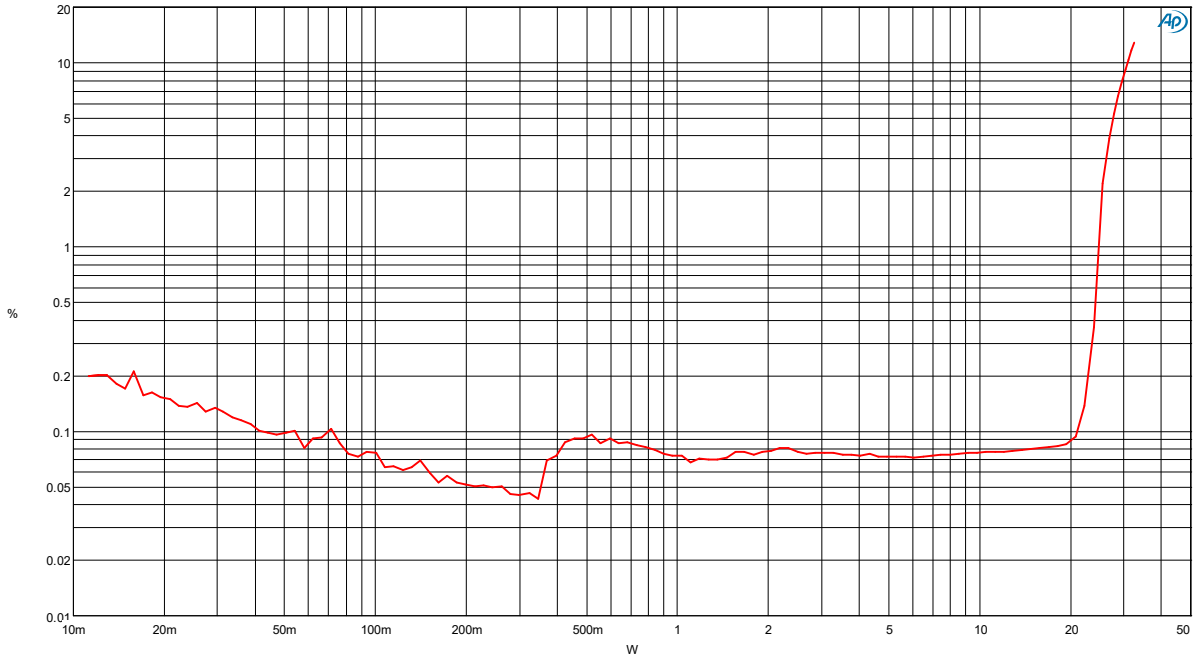
P_O vs η



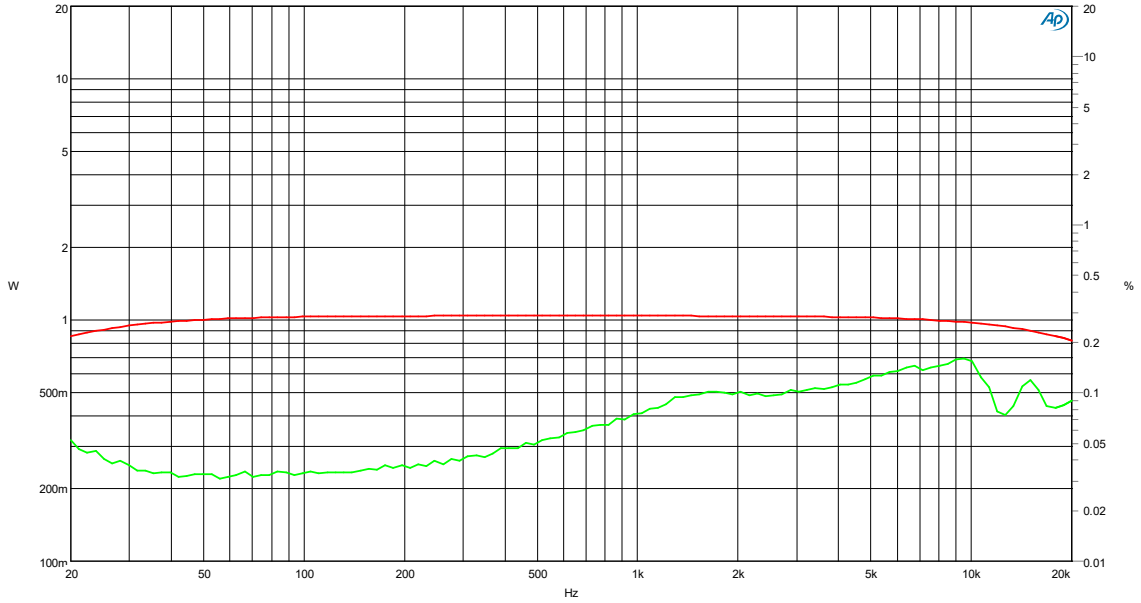
PBTL



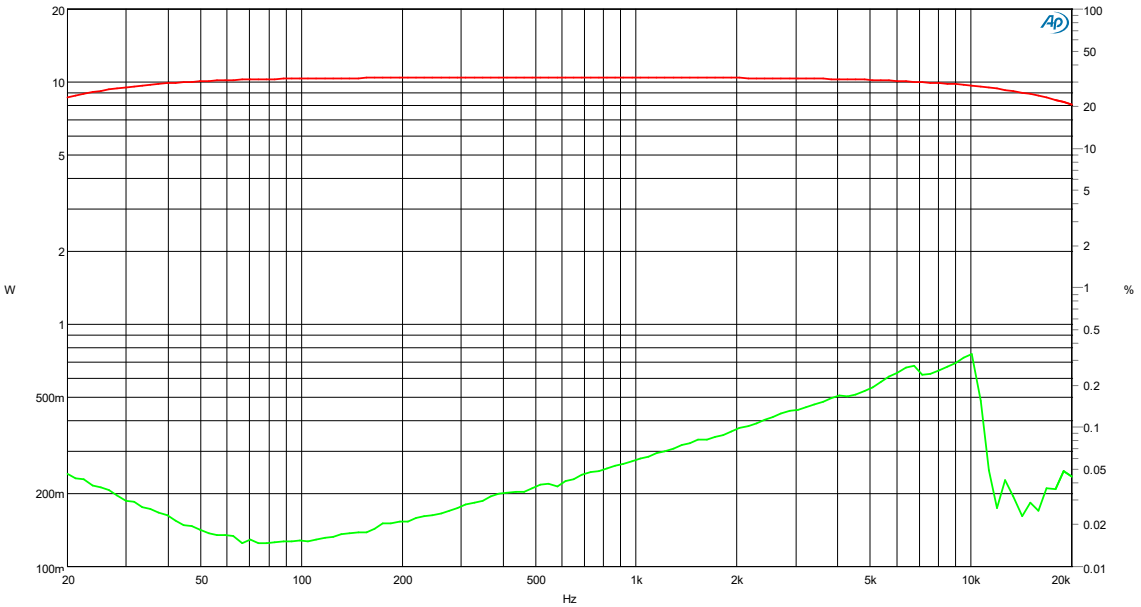
Output Power vs THD+N(PVDD=12V)



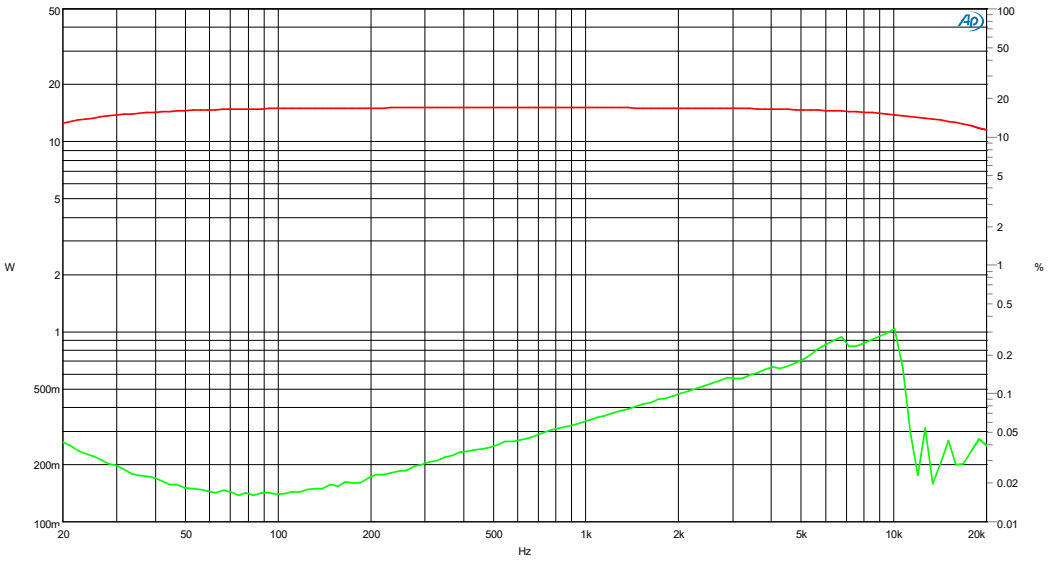
Output Power vs THD+N(PVDD=15V)



f_{IN} vs THD+N(Po=1W)

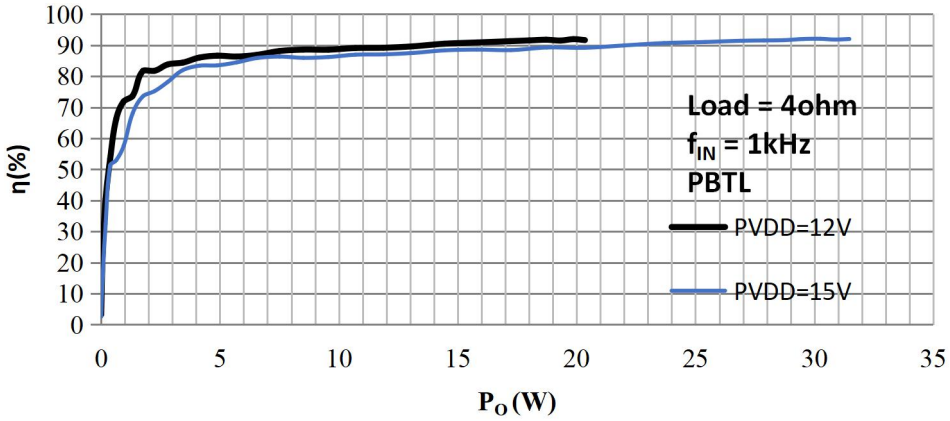


f_{IN} vs THD+N(Po=10W)

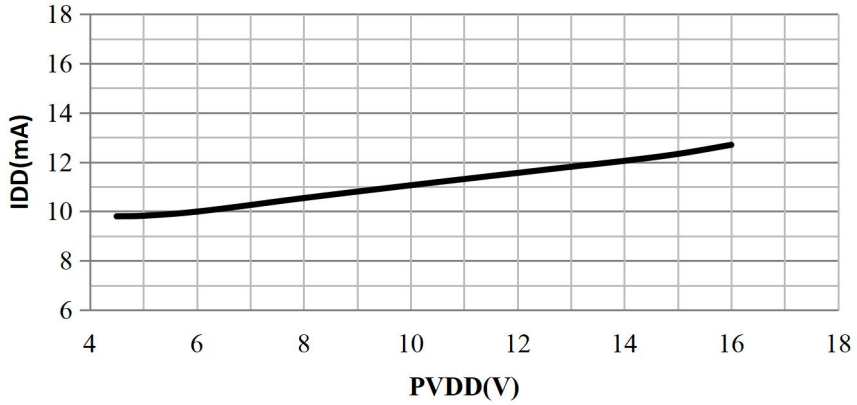


f_{IN} vs THD+N(PVDD=15V,Po=10W)

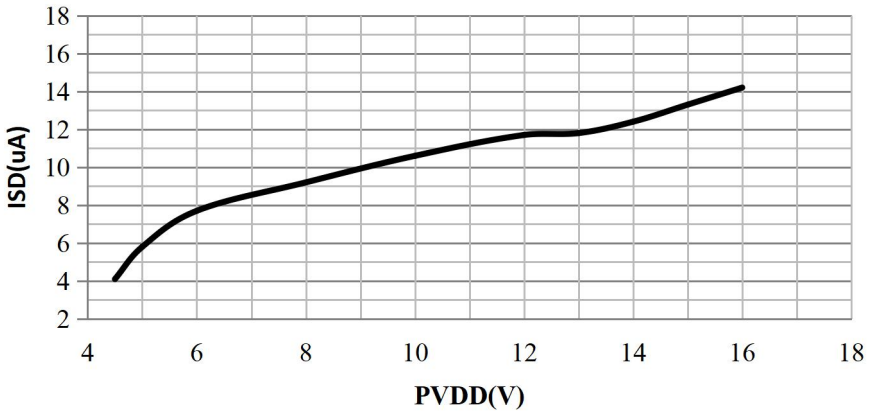
P_O vs η



IDD vs PVDD



ISD vs PVDD



■ APPLICATION INFORMATION

1. Power Supply

The power supply for the HT368 only require one voltage from 4.5V to 16V, which supplies the analog circuitry and the power stage

The AVDD supply feeds internal LDO including GVDD. This LDO output is connected to external pins for filtering purposes, but should not be connected to external circuits. The filtering capacitor for GVDD is recommended to be 1uF.

The PVDD (pin27/pin28) feeds the power stage of L channel and the PVDD (pin14/pin15) feeds the power stage of R channel. Filtering capacitors of 100nF//1uF//220uF for PVDD of each channel should be placed close to the PVDD pin.

2. Amplifier Input and Output

2.1 Amplifier Input Configuration

HT368 is an amplifier with analog input (single-ended or differential). For a differential operation, input signals into IN+ and IN- pins via DC-cut capacitors (C_{IN}). The high pass cut-off frequency of input signal can be calculated by $f_c = \frac{1}{2\pi(External\ R_{IN}+Internal\ R_{IN})\times C_{IN}}$. The input signal gain is calculated by $Gain \approx R_F/(External\ R_{IN}+Internal\ R_{IN})$. The inter RF=400k, inter Rin=10k when GAIN=H,inter Rin=52.7k when GAIN=L.

For a single-ended operation, input signals to IN+ pin via a DC-cut capacitor (C_{IN}). IN- pin should be connected to ground via a DC-cut capacitor (with the same value of C_{IN}).

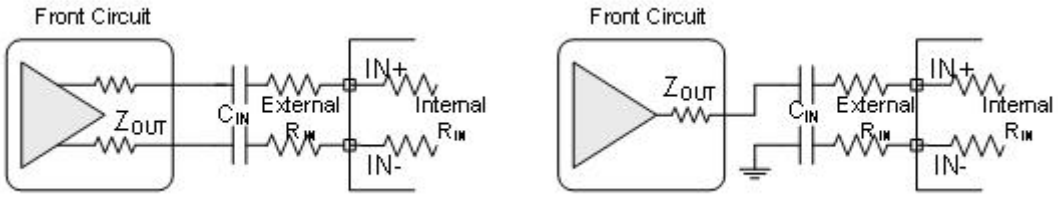


Figure 1 (1) Differential Input; (2) Single-ended Input

2.2 Amplifier Output Configuration

The HT368 has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 20 cm and high power. One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the class-D amplifier. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10 MHz. Also, the filter capacitor can be increased if necessary, with some impact on efficiency.

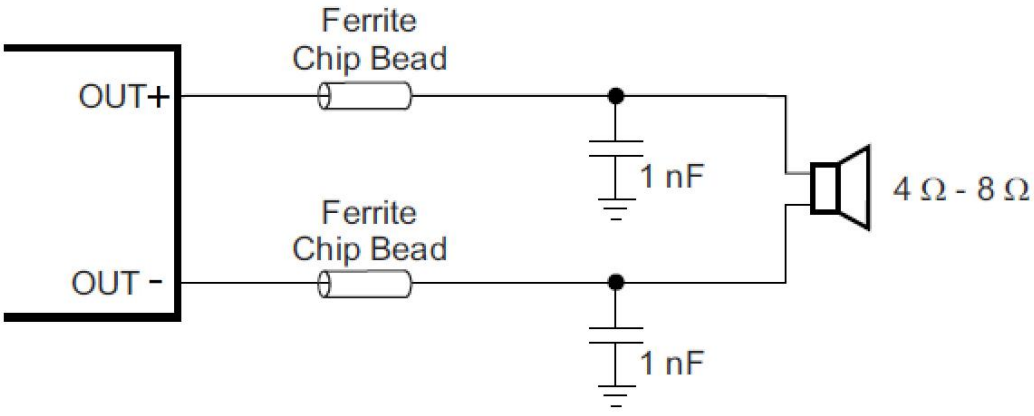


Figure 2 Output Filters with Ferrite Beads

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases, a classic second order Butterworth filter similar to those shown in the figures below can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.

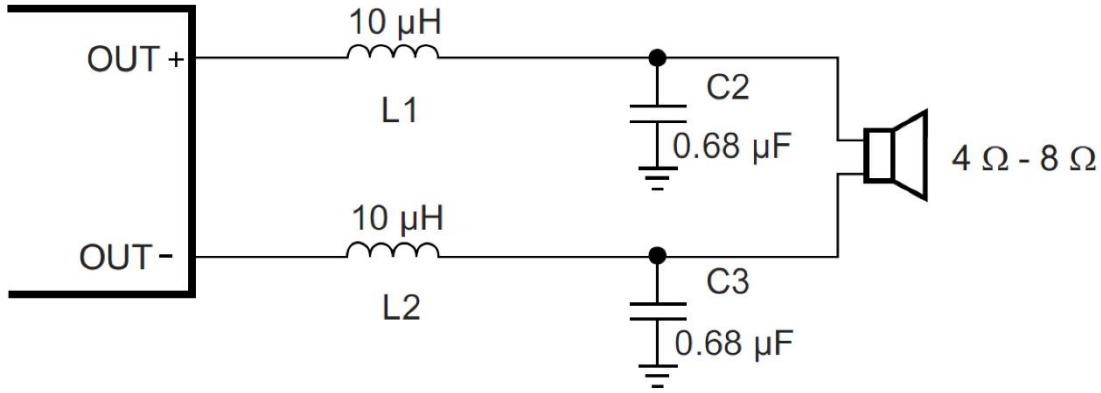


Figure 3 Output Filters with LC

2.3 PBTL Mode Configuration

The HT368 can be configured to drive a single speaker with the two output channels connected in parallel. This mode of operation is called Parallel Bridge Tied Load (PBTL) mode. This mode of operation effectively reduces the output impedance of the amplifier in half, which in turn reduces the power dissipated in the device due to conduction losses through the output FETs. Additionally, since the output channels are working in parallel, it also doubles the amount of current the speaker amplifier can source before hitting the over-current error threshold.

To place the HT368 into PBTL Mode, the LINP and LINN pin should be directly connected to Ground. When operated in PBTL mode, the output pins should be connected as shown in the Typical Application Circuit Diagrams.

In PBTL mode, the amplifier accepts its source signal from the R channel of the stereo signal.

3. Startup, Shutdown

The HT368 employs a shutdown mode of operation designed to reduce supply current (I_{DD}) to the absolute minimum level during periods of nonuse for power conservation. The \SD input terminal should be held high during normal operation when the amplifier is in use. Pulling \SD low will put the outputs to mute and the amplifier to enter a low-current state. It is not recommended to leave \SD unconnected, because amplifier operation would be unpredictable.

For a better power on and power-off pop performance, place the amplifier in the shutdown mode prior to delivering or removing the power supply.

4. Spread Spectrum and De-Phase Control

The HT368 device has built-in spread spectrum control of the oscillator frequency and de-phase of the PWM outputs to improve EMI performance. The spread spectrum scheme is internally fixed and by setting the SD pin above 2.5V to turn on.

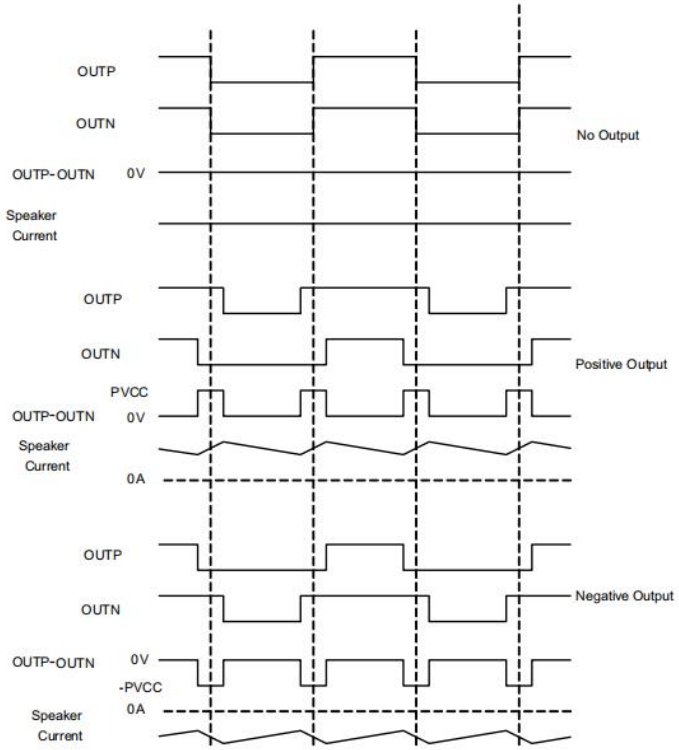
De-phase inverts the phase of the output PWM such that the idle output PWM waveforms of the two audio channels are inverted. De-phase does not affect the audio signal, or its polarity. De-phase only works with BD mode, it is auto-disabled in 1SPW mode

5. Device Functional Modes

MODE=L, BD modulation

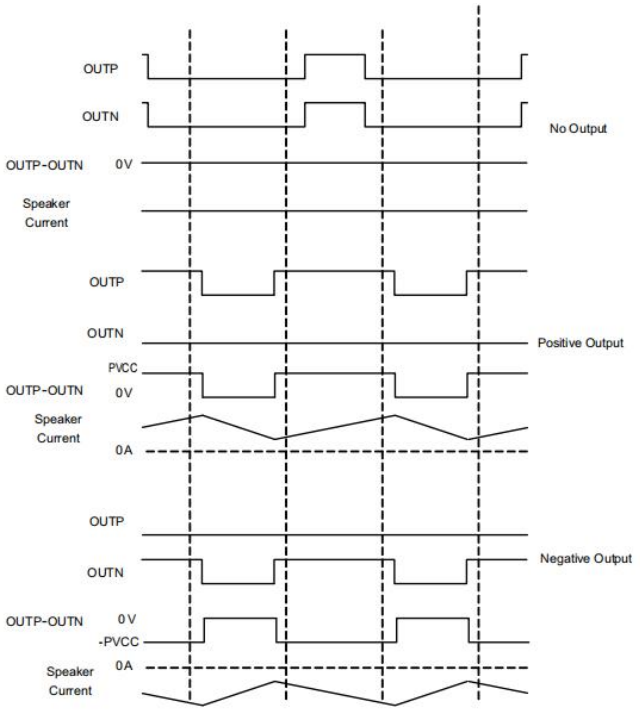
This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving

an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTP and OUTN are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.



MODE=H, 1SPW modulation

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In 1SPW mode the outputs operate at ~15% modulation during idle conditions. When an audio signal is applied one output decreases and the other output increases. The decreasing output signal rails to GND. At which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses.



6. Other Functions and Terminals

6.1 GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. Decouple GVDD with a X5R ceramic 1 μF capacitor to GND. The GVDD supply is not intended to be used for external supply.

6.2 BSPx and BSNx Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220nF ceramic capacitor of quality X5R or better, rated for at least 16 V, must be connected from each output to its corresponding bootstrap input. The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

7. Protection Functions

The HT368 contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against any kind of permanent failures due to short circuits, overload, over temperature, under-voltage, and over-voltage.

7.1 Over Temperature Protection (OTP)

This is the function to establish the over temperature protection mode when detecting excessive high temperature of HT368. When the on-die temperature of HT368 is higher than TOP, the OTP mode is activated, the differential output pin becomes weak low state (a state grounded though resistivity), and the SD/FAULT pin is pulled low.

7.2 DC Detect Protection (DCP)

The HT368 has circuitry which will protect the speakers from DC current which might occur due to an internal amplifier error. A DC detect fault will be reported on the SD/FAULT pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z.

A DCE event occurs when the output differential duty-cycle of either channel exceeds 60% for more than 420 msec at the same polarity. The table below shows some examples of the typical DCE Protection threshold for several values of the supply voltage. This feature protects the speaker from large DC currents or AC currents less than 2 Hz.

7.3 Short-Circuit Protection (OCP) and Automatic Recovery

The HT368 has protection from over current conditions caused by a short circuit on the output stage. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The short circuit

protection fault is reported on the SD/FAULT pin as a low state.

When OCP or OTP or DC error is detected, the SD/FAULT pin will be pulled low. Because the SD input is low, it clear the error signal. Delay a ton time(normal 1.3s), HT368 will try restart.

7.4 Under-Voltage Protection (UVP)

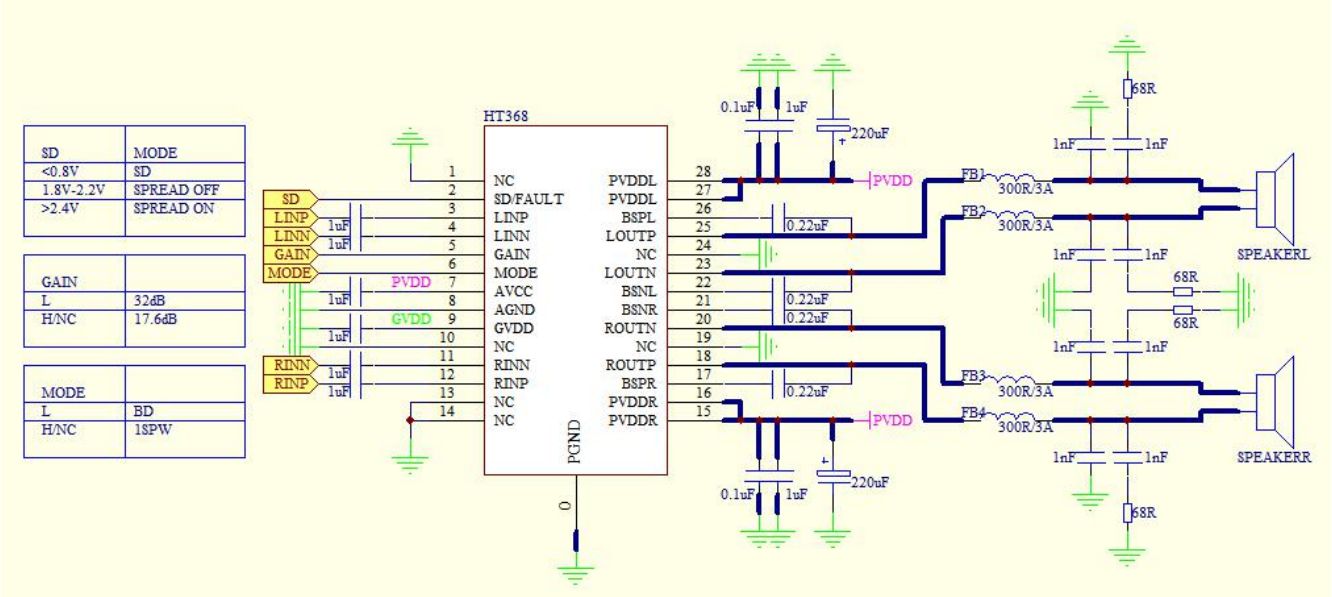
This is the function to establish the under-voltage protection mode when power supply becomes lower than the detection voltage V_{UVLL}, and the protection mode is canceled when the power supply becomes higher than the threshold voltage V_{UVLH}. In the under-voltage protection mode, the differential output pin becomes weak low state (a stage grounded through resistivity). HT368 will start up within start-up time when the under-voltage protection mode is cancelled.

7.5 Uver-Voltage Protection (OVP)

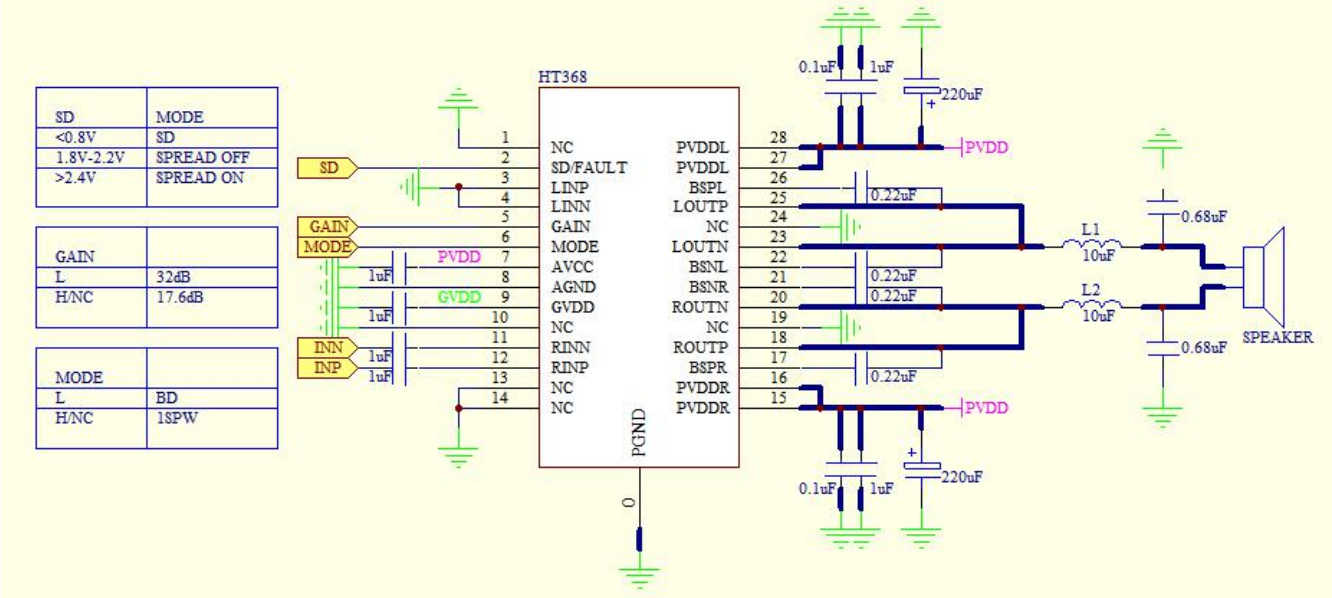
The HT368 device monitors the voltage on PVDD voltage threshold. When the voltage on PVDD pin exceeds the over-voltage threshold (18V typ), the OVP circuit puts the device into shutdown mode. The device recovers automatically once the over-voltage condition has been removed.

8. Typical Applications

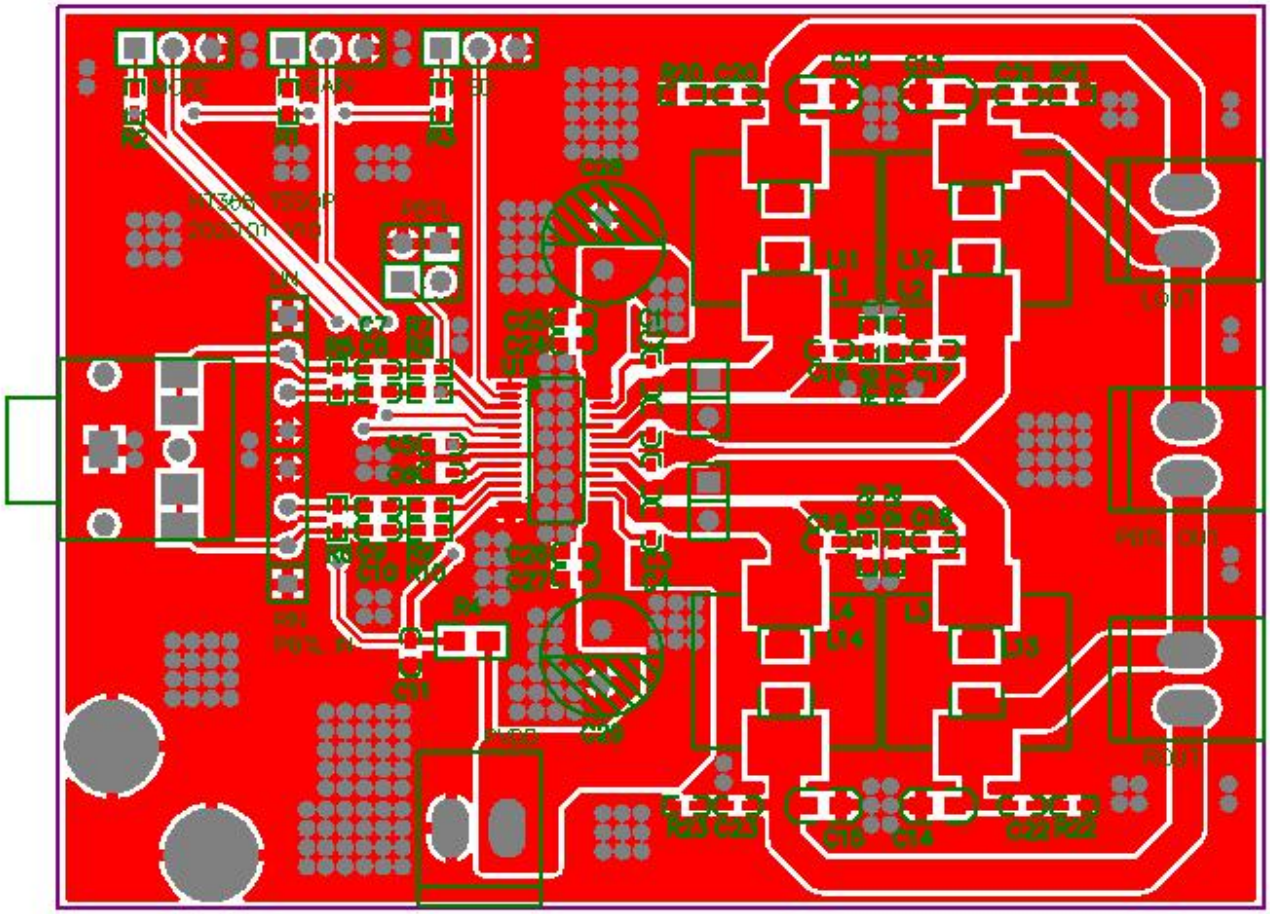
8.1 BTL Mode

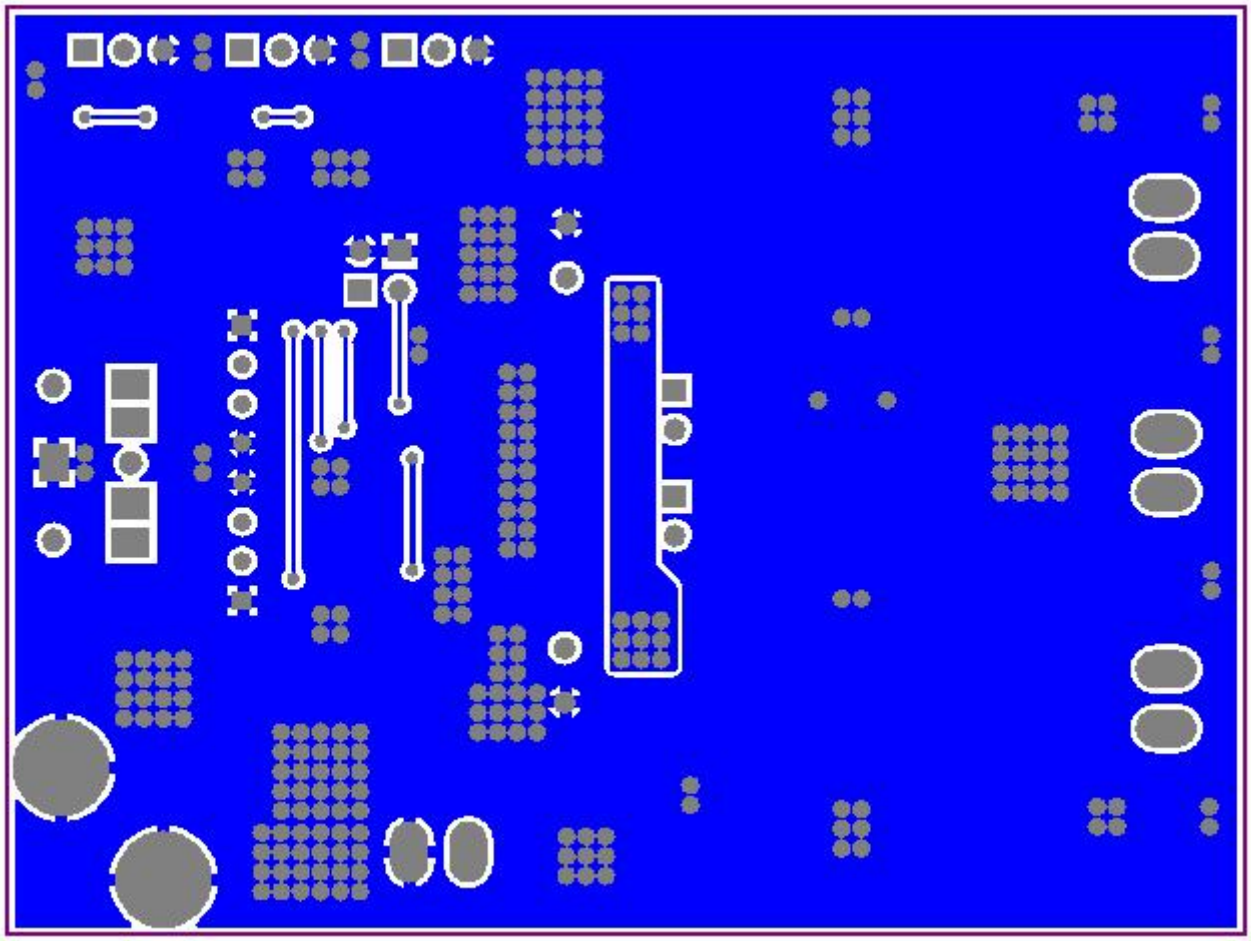


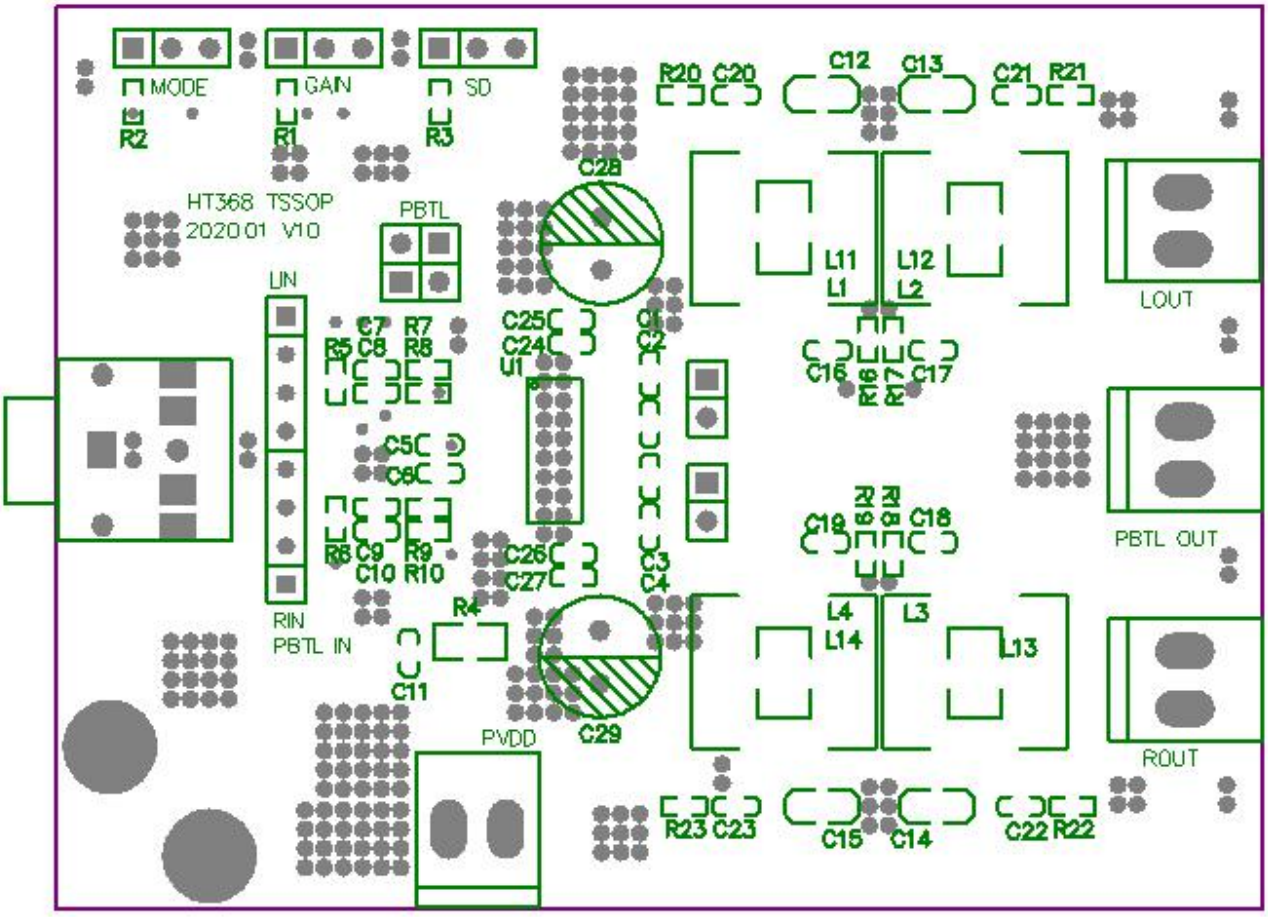
8.2 PBTL Mode



9. PCB Layout

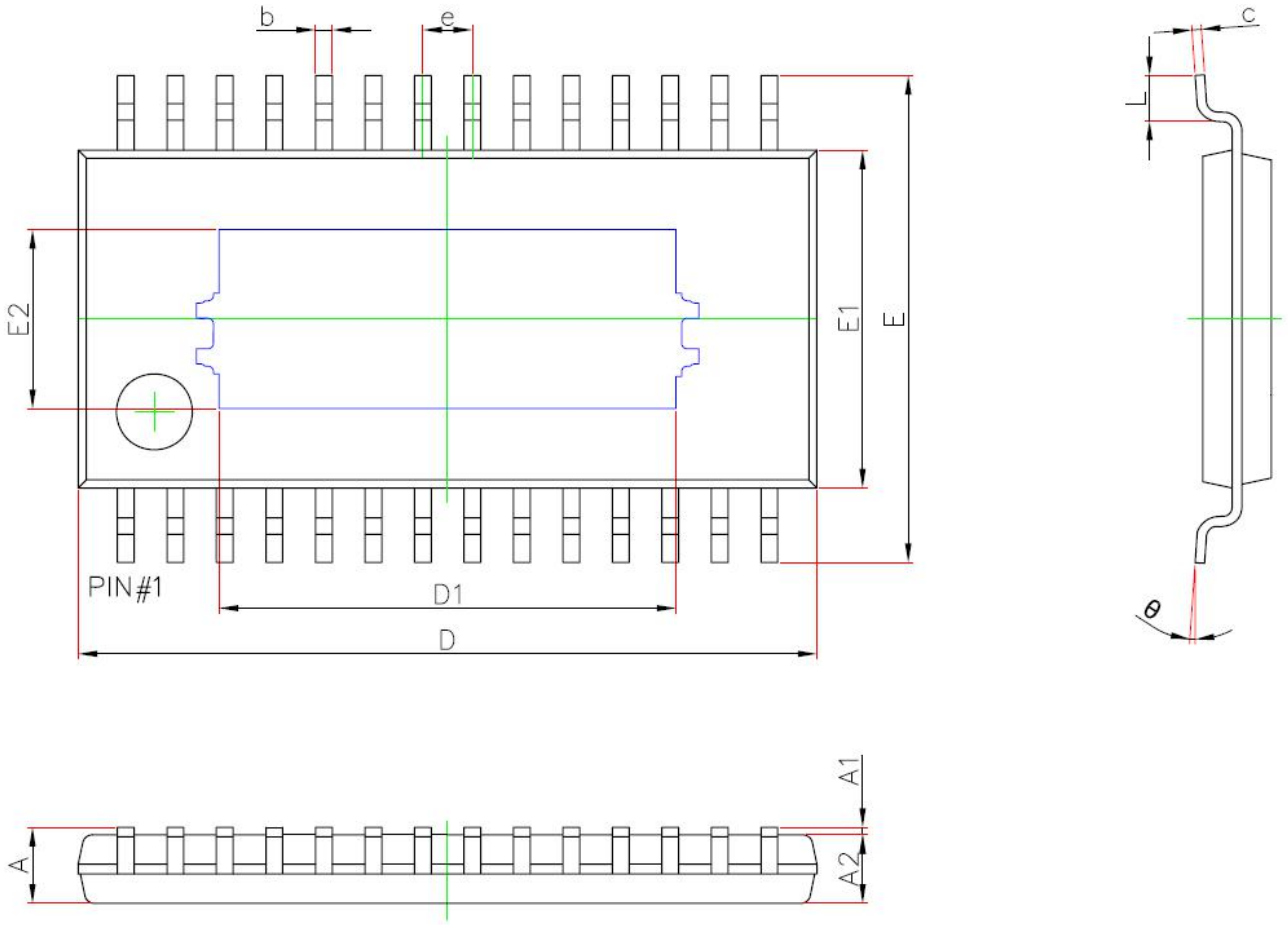





MODE
GAIN
SD
R2
R1
R3
HT368 TSSOP
2020 01 V10
PBTL
LIN
RIN
PBTL IN
PVDD
LOUT
PBTL OUT
ROUT
C28
C29
C12
C13
C20
R20
C21
R21
L11
L12
L1
L2
C16
C17
C18
C19
L4
L3
L14
L13
C15
C14
C22
R22
C23
R23
C11
R4
C26
C27
C25
C24
U1
C7
C8
R5
R7
R8
C5
C6
R6
C9
C10
R9
R10

■ PACKAGE OUTLINE

TSSOP28L-PP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	—	1.200	—	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
D1	5.908	6.108	0.233	0.240
E	6.250	6.550	0.246	0.258
E1	4.300	4.500	0.169	0.177
E2	2.253	2.453	0.089	0.097
e	0.650(BSC)		0.026(BSC)	
L	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°